AF
IEW

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants: M. A. Fathimulla, *et al.*	I hereby certify that this paper is being deposited with the United States Postal Service as first class mail, postage pre-paid, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date:
Serial No.: 10/764,938	
Filed: January 26, 2004	
For: **SILICON-ON-INSULATOR WAFER FOR RF INTEGRATED CIRCUIT**	
Group Art Unit: 2814	
Attorney Docket: H0002270 DIV	May 18, 2006 (Date)
Examiner: L. Pham	
Confirmation No.: 9312	Trevor B. Joike Reg. No. 25,542 Attorney for Appellants

APPELLANT'S BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the provisions of 37 CFR §41.37, Appellants submit the following brief:

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1. Real Party in Interest

The real party in interest is Honeywell, International of Morristown, NJ.

2. Related Appeals and Interferences

There are no other appeals or interferences known to Appellants, Appellants' legal representatives or assignees which will directly affect or be affected by or have a bearing on the Board's decision in the pending appeal.

3. Status of Claims

Claims 1-6 and 22-35 remain in the application. Claims 1-6 and 32-35 are finally rejected and are appealed. Claims 22-31 are withdrawn from consideration as being directed to a non-elected invention.

4. Status of Amendments

All amendments have been entered.

5. Summary of Claimed Subject Matter

As disclosed on page 6, line 14 through page 7, line 18 of the present application, and as shown in Figure 3, an RF device 10 comprises an integrated circuit 12 that has an RF input 14 and an output 16.

An RF substrate 20 is used during the fabrication of the integrated circuit 12 and is shown in Figure 4. The RF substrate 20 includes a high resistivity polysilicon handle wafer 22, a buried oxide layer 24 formed over the polysilicon handle wafer 22, and a silicon layer 26 formed over the buried oxide layer 24. The silicon layer 26 of the RF substrate 20 is processed to form RF components, such as transistors, capacitors, diodes, varactors, and inductors, incorporated to form the RF device 10.

The polysilicon of the polysilicon handle wafer 22 has a high resistivity ρ such as a resistivity ρ greater than 10^6 Ω-cm. Also, polysilicon is less susceptible to the degradation, such as type conversion, that occurs with the single crystal materials heretofore used in RF devices. Moreover, high resistivity polysilicon suffers less loss of resistivity during processing.

6. Grounds of Rejection to be Reviewed on Appeal

Claims 1-6 and 32-35 are rejected under U.S.C. §103(a) as being unpatentable over the U.S. Patent No. 5,376,579 (hereinafter, "the Annamalai '579 patent") in view of admitted prior art and further in view of U.S. Patent No. 4,905,075 (hereinafter, "the Temple '075 patent").

7. Argument

ANNAMALAI '579 PATENT

The Annamalai '579 patent discloses a process for fabricating a silicon-on-diamond (SOD) structure consisting of a silicon substrate, a thin film of deposited diamond on top of the silicon substrate, and an active silicon layer on top of the diamond film. Devices are fabricated in the active silicon layer. Diamond is used as an electrical insulator as compared with SOI, where silicon dioxide is used as an electrical insulator. The diamond film of the SOD structure has a high electrical resistivity and a high thermal conductivity.

As shown in Figure 1, two epitaxial layers 2 and 3 are grown on a seed silicon wafer 1. The layer 2 is an etch stop layer, and the layer 3 is an undoped

silicon layer used to fabricate MOSFETs or bipolar transistors. A diamond layer 4 is deposited on top of the layer 3, a thin polysilicon layer 5 is deposited on top of the diamond layer 4, and a silicon handle wafer 6 is bonded on top of the polysilicon layer 5.

The seed silicon wafer 1 is then removed, and the etch stop layer 2 is removed. The resulting substrate, turned around, now consists of a silicon substrate 6, a polysilicon layer 5, a diamond layer 4, and an undoped silicon layer 3. Devices can be fabricated in the undoped silicon layer 3. This SOD structure now has a buried diamond layer with silicon on either side.

As shown in Figure 2, a SIMOX wafer 1-2-3 is the starting substrate. The buried oxide 2 is used as the etch stop layer, a diamond film 4 is deposited on top of the silicon layer 3, a thin polysilicon layer 5 is deposited on top of the diamond layer, and a silicon handle wafer 6 is now bonded to the thin polysilicon layer 5. The silicon layer 1 is removed, and the etch stop buried silicon dioxide layer 2 is removed. Devices can be fabricated in the thin silicon layer 3.

Figure 3 is used in the Annamalai '579 patent to show another process of making an SOD structure.

Independent claim 1 is directed to an RF semiconductor device comprising a high resistivity polysilicon handle wafer, a buried oxide layer over the polysilicon handle wafer, and a silicon layer over the buried oxide layer.

In the first Office Action, the Examiner appeared to argue (i) that the Annamalai '579 patent discloses the use of high resistivity polysilicon in

fabricating semiconductor devices in general, (ii) that the present application discloses as "admitted prior art" the prior use of high resistivity GaAs in the fabrication of RF semiconductor devices, and (iii) that the use of the semiconductor device disclosed in the Annamalai '579 patent in RF applications is, therefore, suggested by the "admitted prior art" since both "references" rely on high resistivity materials. The Examiner then concludes on the basis of this suggestion that the use of the device disclosed in the Annamalai '579 patent as an RF semiconductor device would have been obvious.

However, the Annamalai '579 patent mentions nothing about the resistivity of the polysilicon layer 5 and does not disclose or suggest that the polysilicon layer 5 is a high resistivity polysilicon layer.

The Annamalai '579 patent does state that the diamond layer 4 has a high resistivity on the order of 10^{16} ohm-cm. However, independent claim 1 requires a high resistivity polysilicon handle wafer, not a high resistivity insulating layer.

Accordingly, since neither "reference" relies on high resistivity polysilicon, there is no suggestion to use high resistivity polysilicon for the polysilicon disclosed in the Annamalai '579 patent.

Similarly, as discussed below, the Temple '075 patent does not disclose or suggest the use of high resistivity polysilicon in the fabrication of RF semiconductor devices.

Therefore, there is no suggestion to combine the Annamalai '579 patent, the "admitted prior art," and the Temple '075 patent, and independent claim 1 is

accordingly not unpatentable over the Annamalai '579 patent in view of "admitted prior art."

In the Final Rejection, the Examiner asserted that the fact that the Annamalai '579 patent fails to disclose a high resistivity polysilicon handle wafer is not relevant since the Examiner is relying only on the intermediate structure.

However, this assertion was rather cryptic in that the Examiner does not tell applicants the composition of the intermediate structure.

A first way to read the Examiner's assertion is that the Examiner relied on the structure of Figure 1, 2, or 3 of the Annamalai '579 patent as the intermediate structure since not one of these structures is the final structure, at least in the sense that the layers 1 and 2 must be removed to produce the final structure. However, even in this case, there is no disclosure in the Annamalai '579 patent that the polysilicon layer 5 in any of these "intermediate" structures is high resistivity.

A second way to read the Examiner's assertion is that the Examiner relied on the layers 3-6 as shown in Figure 1 or 2 or the layers 3-5 as shown in Figure 3 of the Annamalai '579 patent as the intermediate structure, and that the final structure is one where the polysilicon layer is replaced by a high resistivity polysilicon layer. In this case, the Examiner must then be asserting that the use of high resistivity GaAs as disclosed in the "Admitted Prior Art" suggests to one of ordinary skill in the art the use of high resistivity polysilicon for the polysilicon shown in the Annamalai '579 patent.

However, the combination of the "Admitted Prior Art" and the Annamalai '579 patent can only at most

suggest substituting high resistivity GaAs for the polysilicon shown in the Annamalai '579 patent. There is no basis in either the Annamalai '579 patent or the "admitted prior art" for suggesting to one of ordinary skill in the art the substitution of high resistivity polysilicon for the polysilicon disclosed in the Annamalai '579 patent.

Moreover, as disclosed in the present application, the use of high resistivity silicon substrates in RF applications was known to be problematical because donors that are thermally generated during post-processing degrade the resistivity both at the SiO_2/Si interface. This degradation produces higher losses, increases coupling (cross-talk), lowers inductor Q, and is not so easily remedied. Therefore, one of ordinary skill in the art would not have looked to silicon as a solution to this degradation problem and instead would have used GaAs.

Accordingly, for both of these reasons, the Annamalai '579 patent and the "Admitted Prior Art" would not have suggested to one of ordinary skill in the art the use high resistivity polysilicon to produce the invention of independent claim 1.

The Temple '075 patent, relied by the Examiner in the rejection of independent claim 1, discloses a semiconductor package 10 for a semiconductor chip 12. The semiconductor package 10 has a high resistivity polysilicon base 15, a high resistivity polysilicon sidewall 20, and a high resistivity polysilicon cover 30. The high resistivity polysilicon base 15 centrally supports the semiconductor chip 12, and an exposed peripheral surface 16 of the base 15 engages the high

resistivity polysilicon sidewall 20. An upper surface 22 of the high resistivity polysilicon sidewall 20 engages a lower surface 28 of the high resistivity polysilicon cover 30.

The high resistivity polysilicon cover 30 includes external terminals 31 and a means to couple a signal between the external terminals 31 and electrodes 13 of the semiconductor chip 12. This means includes a highly conductive region 32 of the high resistivity polysilicon cover 30, a contact washer 25, and a metal 27.

There is no disclosure in the Temple '075 patent that high resistivity polysilicon is used in the fabrication of the semiconductor chip 12, only in the packaging 10 for the semiconductor chip 12. Accordingly, the Temple '075 patent does not suggest to one of ordinary skill in the art fabricating the semiconductor chip disclosed in the Annamalai '579 patent with high resistivity polysilicon.

Consequently, the combination of the Annamalai '579 patent, the "admitted prior art,", and the Temple '075 patent would not have suggested to one of ordinary skill in the art the fabrication of a semiconductor chip with high resistivity polysilicon. Therefore, independent claim 1 is not unpatentable over the Annamalai '579 patent in view of "admitted prior art" and further in view of the Temple.

In the Advisory Action, the Examiner first argues that the term "high resistivity" is a relative term and, as such, the Examiner apparently ignores the high resistivity limitation of independent claim 1. However, the term "high resistivity" must mean something

in independent claim 1 because words in a claim cannot be totally ignored. Therefore, whatever meaning that is given to the term "high resistivity," it is clear that the Annamalai '579 patent does not meet this term because the Annamalai '579 patent ascribes no resistivity to its polysilicon and, therefore, the cannot disclose a high resistivity polysilicon.

Moreover, the term "high resistivity" is a well understood term in the art as exemplified by the claims 8 and 18 of the Temple '075 patent. Certainly, both the inventors and the Examiner of that patent understood the term "high resistivity."

Accordingly, because term "high resistivity" cannot be ignored, and because none of the prior art relied on by the Examiner discloses or suggests the use of high resistivity polysilicon in an RF device, independent claim 1 is patentable over the Annamalai '579 patent in view of admitted prior art and further in view of the Temple '075 patent.

Also in the Advisory Action, the Examiner states that the Temple '075 patent is being relied on to show a high resistivity polysilicon handle wafer. However, the Temple '075 patent does not disclose a high resistivity polysilicon handle wafer. Instead, the Temple '075 patent merely shows high resistivity polysilicon packaging. Accordingly, the Temple '075 patent does not suggest the use of high resistivity polysilicon in the SOI stack recited in independent claim 1.

Independent claim 3 is directed to an RF semiconductor device comprising a high resistivity polycrystalline layer, a buried oxide layer over the

polycrystalline layer, and a silicon layer over the buried oxide layer.

As should be clear from the discussion above, the Annamalai '579 patent, "admitted prior art" prior are, and the Temple '075 patent doe not disclose or suggest the use of a high resistivity polycrystalline material in the SOI stack recited in independent claim 3.

Accordingly, independent claim 3 is not unpatentable over the Annamalai '579 patent in view of "admitted prior art" and further in view of the Temple '075 patent.

Because independent claims 1 and 3 are not unpatentable over the Annamalai '579 patent in view of admitted prior art and further in view of the Temple, dependent claims 2, 4-6, and 32-35 are likewise not unpatentable over the Annamalai '579 patent in view of admitted prior art and further in view of the Temple '075 patent.

Moreover, dependent claims 32 and 34 recite that the high resistivity polysilicon or polycrystalline handle wafer comprises a high resistivity polysilicon or polycrystalline handle wafer having a resistivity ρ greater than 10^6 Ω-cm. The art applied by the Examiner does not show a polysilicon or polycrystalline handle wafer having this resistivity.

Moreover, the Temple '075 patent discloses the use of high resistivity polysilicon in packaging a semiconductor device but does not disclose or suggest the use of high resistivity polysilicon in the fabrication of the semiconductor device itself as required by the claims of the subject application. Therefore, the Temple '075

patent cannot suggest the invention of dependent claims 32 and 34 to one of ordinary skill in the art.

Accordingly, dependent claims 32 and 34 are patentable over the Annamalai '579 patent in view of "admitted prior art" and further in view of the Temple '075 patent.

Dependent claims 33 and 35 recite that the silicon layer comprises an RF processed silicon layer. The art applied by the Examiner does not show an RF processed silicon layer.

The Examiner gives no weight to a limitation of a claim, thereby again conveniently ignoring a limitation for which the Examiner has cited no art.

In the specific case at hand, the Examiner essentially argues that the limitation RF processed silicon layer is a processing step rather than a structural limitation. However, the limitation RF processed silicon layer is not a processing step and, therefore, cannot be ignored.

Accordingly, dependent claims 33 and 35 are patentable over the Annamalai '579 patent in view of admitted prior art and further in view of the Temple '075 patent.

8. Claims Appendix

An appendix containing the rejected claims is attached.

9. Evidence Appendix

There is no submitted evidence. Therefore, there is no corresponding appendix.

10. Related Proceeding Appendix

There are no related proceedings. Therefore, there is no corresponding appendix.

11. Conclusion

For the foregoing reasons, reversal of the Final Rejection is respectfully requested.

The fee set forth in 37 C.F.R. §41.20 is enclosed.

Respectfully submitted,

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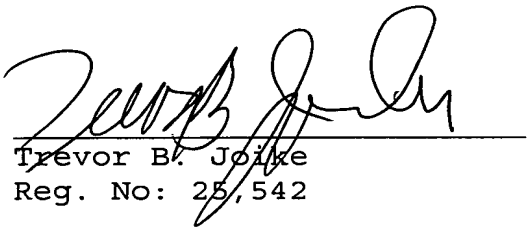
By: 

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May 18, 2006

APPENDIX

1. An RF semiconductor device comprising:

a high resistivity polysilicon handle wafer;

a buried oxide layer over the polysilicon handle wafer; and,

a silicon layer over the buried oxide layer.

2. The RF semiconductor device of claim 2 further comprising an RF input.

3. An RF semiconductor device comprising:

a high resistivity polycrystalline layer;

a buried oxide layer over the polycrystalline layer; and,

a silicon layer over the buried oxide layer.

4. The RF semiconductor device of claim 3 wherein the polycrystalline layer comprises a polysilicon layer.

5. The RF semiconductor device of claim 3 further comprising an RF input.

6. The RF semiconductor device of claim 5 wherein the polycrystalline layer comprises a polysilicon layer.

32. The RF semiconductor device of claim 1 wherein the high resistivity polysilicon handle wafer comprises a high resistivity polysilicon handle wafer having a resistivity ρ greater than 10^6 Ω-cm.

33. The RF semiconductor device of claim 1 wherein the silicon layer comprises an RF processed silicon layer.

34. The RF semiconductor device of claim 3 wherein the high resistivity polycrystalline handle wafer comprises a high resistivity polycrystalline handle wafer having a resistivity ρ greater than 10^6 Ω-cm.

35. The RF semiconductor device of claim 3 wherein the silicon layer comprises an RF processed silicon layer.